anticipated baud rate of the incoming signal and to optimize the signal quality and the quality of the received data.

Signal quality is adversely affected by both intersymbol interference (ISI) and adjacent channel interference (ACI). Analog filtering circuits are commonly applied to reduce ISI, ACI, or other electronic noise associated with digital signal transmissions. ISI is reduced when the filter bandwidth is widened and ACI is reduced when the bandwidth is narrowed. Unfortunately, conventional fixed bandwidth filters inherently increase the amount of ISI when they are tuned to reduce ACI, and vice versa. As such, conventional analog filtering circuits in digital receivers are usually tuned to a less-than-optimum bandwidth with respect to ISI and ACI, which are often unknown *a priori*.

The bandwidth accuracy of conventional tunable analog filters is only about 10%. Although such accuracy may be sufficient to enable a digital receiver to gain symbol synchronization, the bandwidth inaccuracy may produce an unacceptable bit error rate (BER) resulting from excessive ISI or ACI. To minimize the BER in some applications, it may be necessary to maintain bandwidth accuracy to within 5% or less. Unfortunately, conventional fixed bandwidth filters are not responsive to fluctuations in BER, ISI, or ACI.

We will now consider in detail the effects of the different noise sources on the signal, when viewed over a short period of time, that is, without environmental changes. For clarity and ease of understanding, this field is described using elementary probability theory, which is a tool used widely in the engineering management of these problems. This theory is often taught pre-university, and expanded as a first year introductory topic for electronic engineering courses, and those versed in the field will be intimately familiar with this.

Data errors in a channel with Gaussian distributed phase and amplitude noise can be considered as a noiseless ideal channel and with noise assigned to a clock signal, which gives rise to the probability distribution of the sampling point as shown in Fig.3. Symbols S0, S1 and S2 represent symbols on the input of the receiver, which samples the data at a point in time which is symmetrically distributed around the moment x according to Gaussian distribution and described by the formula:

$$\rho(t) = \frac{1}{\sqrt{\pi}} e^{\frac{(t-x)^2}{\sigma^2}}$$

So here we have a channel, with three subsequent symbols, S0, S1, and S2. In Figure 3, the distribution in time of the sampling point for S1 is shown, but in reality, each symbol has a similar curve, so we can consider the data stream as a series of symbols, each of which is sampled by a series of distributions. This is shown clearly in Figure 5.

The Bit error rate (BER) can be calculated as a probability to sample the wrong symbol and it is equal to probability to sample other than S1 channel symbol (dashed area in Figure 3) multiplied by the probability that symbol S1 has a different value, which for binary coding with equally distributed zeros and ones is equal to 0.5. This can be described by the formula:

$$BER(x) = \frac{1}{2\sqrt{\pi}} \left(\int_{-\infty}^{0} e^{-\frac{(t-x)^2}{\sigma^2}} dt + \int_{1}^{\infty} e^{-\frac{(t-x)^2}{\sigma^2}} dt \right) = \frac{1}{4} \left[erfc\left(\frac{x}{\sigma}\right) + erfc\left(\frac{1-x}{\sigma}\right) \right]$$

For the distribution shown in Fig.3, the BER function is shown in Fig. 4.

The BER curve has a minimum in the middle of bit interval, as shown in Figure 4 for one symbol. For a series of symbols, this BER curve becomes a periodic function with a period equal to one bit interval. This is shown in Fig.5.

The value at the minimums depends on the distribution width σ. A graph of resulting function is shown in Fig. 6.

The signal to noise ratio can be calculated in dB, for bit width w and RMS jitter according to the formula:

$$SNR = 20 \lg\left(\frac{w}{2\sigma}\right)$$

For a single flip-flop, the probability to capture a logic state (either from a 0 to a 1, or a 1 to a 0) is a function of the time difference between the sampling point and the point where input signal crosses the threshold. This function can be approximated as following:

$$P(x) = \frac{1 + Erf(\frac{x}{\sigma})}{2}$$

where P(x) is a probability to capture the correct logic state,

x is a time difference between the moment when the input signal crosses the threshold and the sampling point,

σ is the RMS value of noise in a system, that is the congregate of noise in channel, driver and receiver.

Fig.7 is a diagram showing a plot of this probability function taken from an interface implemented using SSTL16857 registers as the solid line, and the theoretical function as the dotted line. In this case, the value of σ is 21 pico seconds, from observation of the measured signal with its noise. This distribution is $P(x) = 1 - P(-x)$.

In addition to the noise distribution of the signal, we must consider the effect of environmental changes, which cannot be considered by the same BER analysis, because the time period needed to consider the environment is of many orders of magnitude longer than the time period involved in the consideration of phase and channel noise.

In a communication channel, the integrity of the received data can be observed using an eye diagram, such as in Fig. 2. The eye in the very centre is the region where the data is stable and is strobed. The eye diagram shows time in the X domain, in picoseconds in Fig. 2, and voltage or current in the Y domain, in mV in Fig.2. To receive the data correctly, it is necessary to sample the data (e.g. by closing a gate in the time domain), with the switching threshold of the gate as close as possible to the centre of the eye. A technique for tracking the centre of the eye in the voltage or current domain is described in US patent application 60/315,907. The present invention relates to how the eye is tracked in the time domain.

The problem addressed by this innovation arises in very high speed systems, where each signal can move in time due to changes in the environment, in addition to movement due to channel noise, as has been already considered. For example, if a

same instant in time, their internal phase noise will cause them to latch at different points in time, as a function of the distribution which is shown in Fig. 3.

In a more refined embodiment, the present invention spaces the plurality of registers in time using delay elements, or wire with inherent delay, and then applies the outputs of these registers to a logic network to determine which register has the lowest bit error rate. This set of delay elements can be implemented using a polyphase clock generator to equalise the space between registers.

Thus, in one aspect of the invention, a receiver is provided, comprising a plurality of samplers for sampling data, coupled with a set of delay devices for providing a series of signal copies with each copy being shifted by a predetermined time interval, at least one means for comparing signals latched by said samplers, a means, such as multiplexer, for choosing a signal copy with minimal BER, and a means, such as state machine, for determining the number of the signal copy with minimal BER, and optionally, a pipeline for latency adjustment.

In another aspect of the invention, a receiver comprises a plurality of samplers for sampling data, providing a series of simultaneous signal copies, at least one means for comparing signals latched by said samplers, a means for choosing a signal copy with minimal BER, a means for determining the number of the signal copy with minimal BER, and optionally, a pipeline for latency adjustment.

In still one more aspect of the invention, a receiver comprises at least one sampler for sampling data coupled with a set of delays, or a variable delay, providing a series of spaced in time signal copies, at least one means for comparing signal copies, a means for selecting a signal copy with minimal BER, a means for determining the delay corresponding to this copy, and a means for applying the obtained delay to other samplers when sampling data.

The proposed receiver provides the high speed transmission of data, wherein the data transmitted are latched at the moment when the signal has the maximal stability.

Preferably, the samplers are implemented as registers, flip-flops, latches, track-and-hold, sample-hold devices, etc.

When the sampler inherent noise is negligible, the number of samplers used for majority function does not make any significant changes in resulting BER as seen in Fig.7.

Averaged and normalized E output of majority element also does not significantly depend on the number of majority element inputs as shown in Fig. 8.

From the expectation that the largest portion of noise belongs to driver, channel media and clock generator, it is clear that it is preferable to use minimum number of inputs at majority elements which is 3.

The resulting BER value is different for different number of samplers equally distributed across bit interval and for different ratio between bit interval and RMS noise value. These functions are presented in Fig.9, where the number of samplers is on horizontal axis and the ratio between bit interval and σ is an index of BER function. It is clear from this picture that the optimal number of samplers per bit is close to 16.

A simplified alternative arrangement is shown in Fig. 8. According to this embodiment, a single bit receiver contains three monotonic delay verniers 61, 62, 63, transition 66, two samplers 64, 65 with pipeline adjusters 67, 68, controller 69 and output multiplexer 70.

The feedback loop or detector 66 is used to control the best sampling point position. For example this detector can be implemented as shown in Fig.11. Two independent flip-flops 11, 12 are sampling of their inputs simultaneously. Each flip-flop is defined by the P(x) function described above.

The state machine 69 continuously scans the vernier 63 at the input of the transition detector 66 and measures and keeps values corresponding to the minimums of that function. The preferable range of these verniers should not be less than two channel symbol intervals to allow have more than one local minimum. Scanning need only be provided at a low frequency, such as 20KHz, allowing easy filtering of the received data from the transition detector signal. At the end of each cycle of scanning the vernier at the input of transition detector, the co-ordinate of the value closest to the middle minimum is loaded into one of verniers at the input of sampler. Both samplers 64, 65 work consecutively. When scanning is finished and a